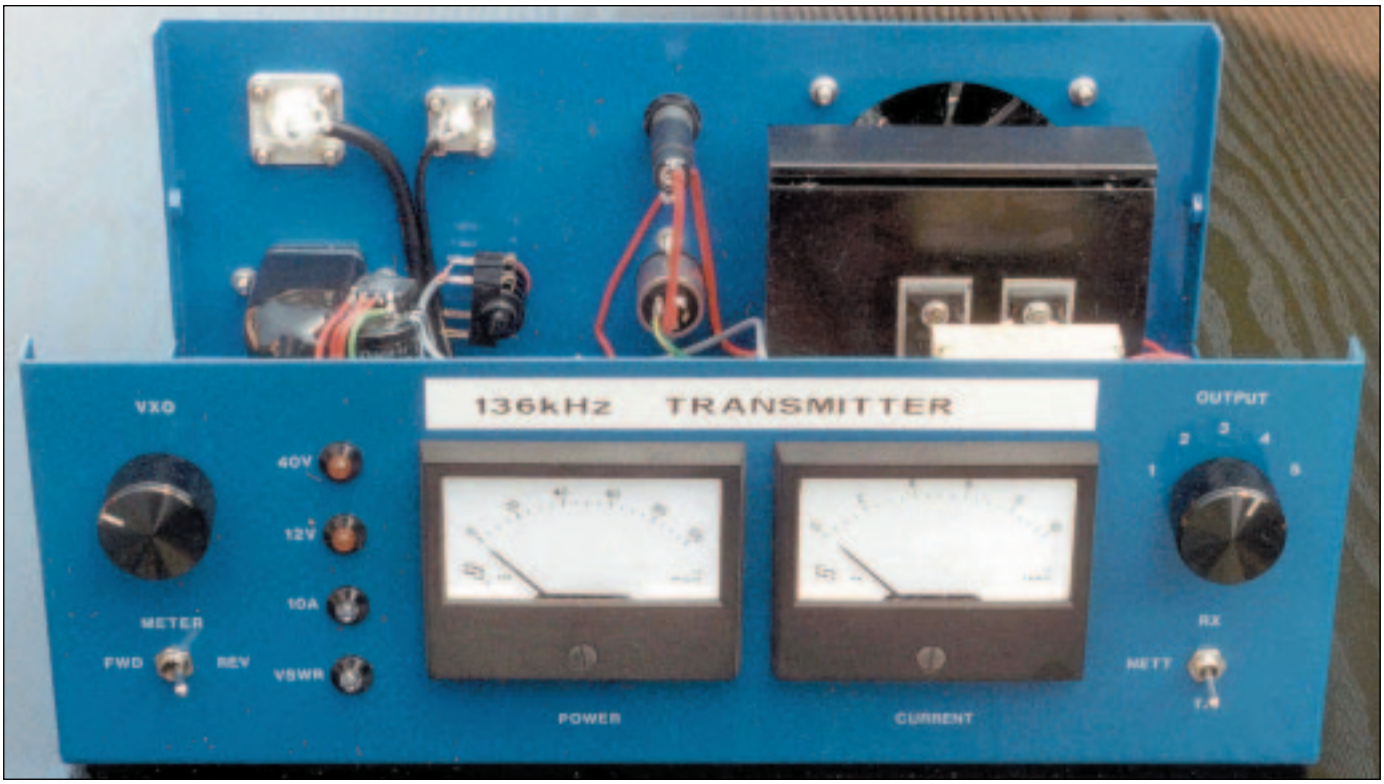
A Class-D Transmitter for 136kHz

Part one of a two-part 300W design by David Bowman, G0MRF *



The completed 136kHz transmitter, with its cover removed.

THE 136kHz low-frequency allocation was announced in the UK in February 1998. In the intervening five years, LF has been introduced in many countries, and there are now over 30 DXCC entities licensed for 135.7 to 137.8kHz. Several other administrations, including the United States and Canada, are considering similar allocations in the LF region and some have already issued experimental permits.

Initially, there was a degree of scepticism about the distances that could be worked with just 1W of effective radiated power. To put the DX potential into perspective, the Atlantic was first spanned with a cross-band QSO in September 2000 and currently, the two-way record is 5418km between Laurie, G3AQC, and VA3LK.

With no commercial equipment available from the established 'big four' manufacturers, LF designs have relied on individuals bringing a variety of ingenious ideas to the band. This transmitter combines a number of proven techniques and, with over 300W output, allows you to get on to this exciting amateur allocation with a good signal. The transmitter is based around an amplifier using two low-cost power FETs in a high-efficiency class-D configuration. The transmitter is protected against over-current and high-VSWR conditions. The single PCB also includes forward- and reflected-power metering, output filtering and transmit / receive switching.

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CIRCUIT DESCRIPTION

THE TRANSMIT DRIVE is generated by a pair of crystals operating as variable crystal oscillators. Crystal X1 is 8000kHz while Crystal X2 is 8274kHz (see **Fig 1** opposite). Each crystal is connected across a CMOS NAND gate, which functions as an oscillator. Varicap diodes are used for differential-tuning of the crystals. The two outputs are applied to a third NAND gate which, because logic gates are non-linear, functions as a mixer. The output of IC1(c) contains several products including the difference frequency at 274kHz. A low pass filter, comprising L1, C10 and C11, removes the high-order products, leaving a sine wave at twice the required output frequency. The filter is terminated by R7, which is part of the inverting amplifier IC2. C13 in the feedback loop adds some additional low-pass filtering before the signal is applied to the clock input of a 4013 D-type flip-flop. A small PCB jumper provides the option of driving the transmitter from an external source [1].

IC3 has two functions. Firstly, it divides the input frequency by two, producing 136kHz at the (Q) and (not Q) outputs. The second function of IC3 is to act as a switch in the event of a fault condition. In normal operation the Set Direct input, pin 8, is held at 0V by R16. The circuit uses D1 - D3 as a simple discrete OR gate to provide control and protection functions. Diodes D1 and D2

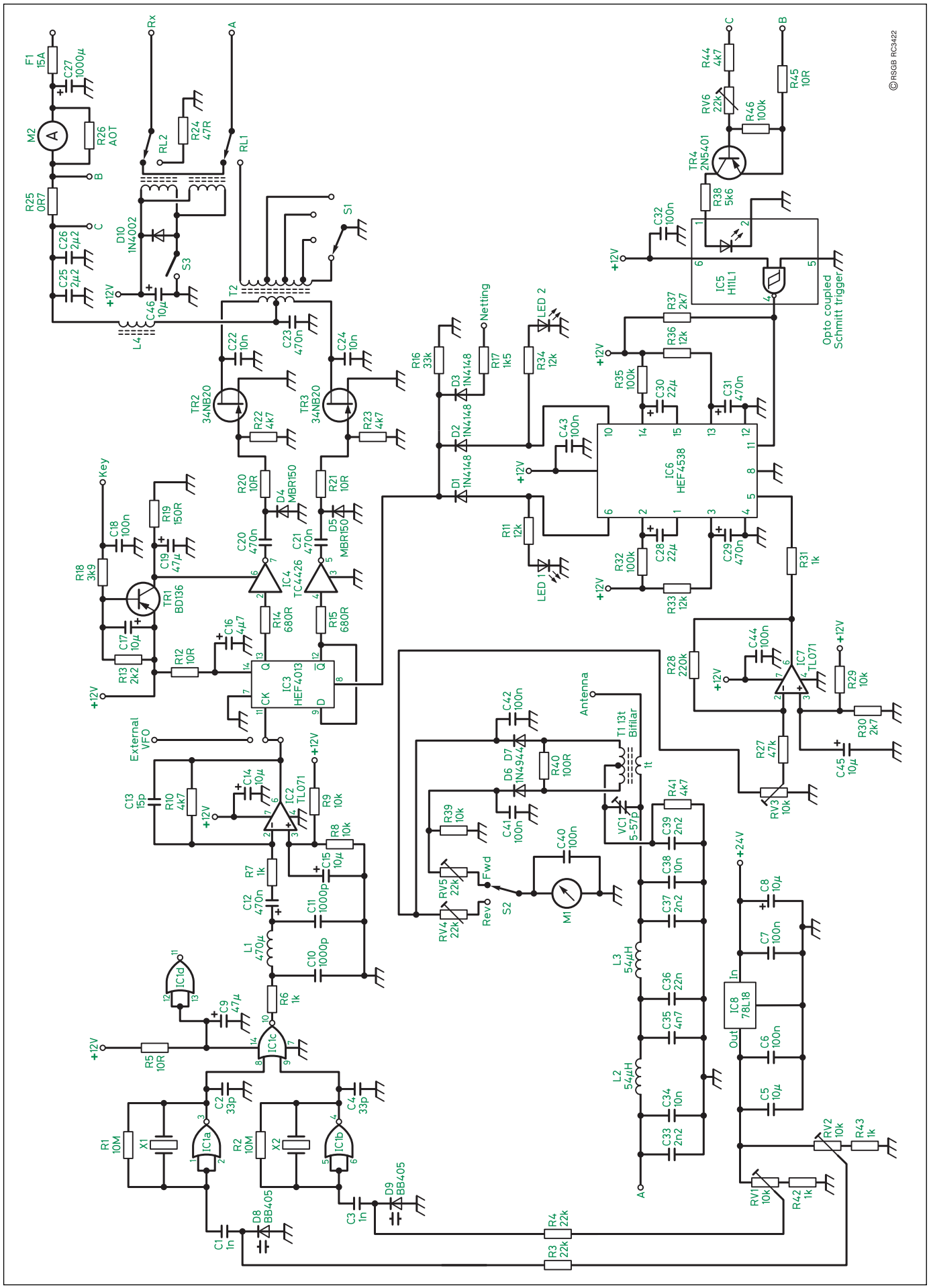

Fig 1: Complete circuit diagram of the 136kHz transmitter.

feed in signals from the reflected power and over-current protection circuits, while D3 is used to provide a netting facility on receive.

If D1 *or* D2 *or* D3 conduct, the Set Direct input will go to 12V, causing IC3 to shut down, removing the drive from the power amplifier. **Fig 2** shows how these functions can be controlled with a double-pole centre-off switch. One pole is used to drive the transmit / receive relays, while the other switches on a cooling fan during transmit periods.

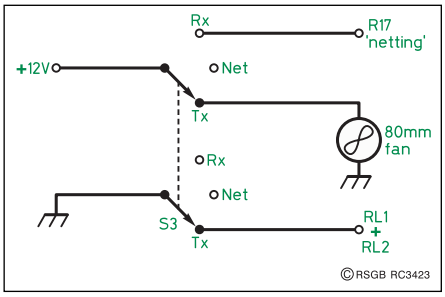

Fig 2: Transmit / receive switching, using a DPDT centre-off switch.

Netting is carried out with the switch in its centre-off position. This puts the relays in the receive position, but keeps the 4013 divider active.

IC4 is a dual-inverting FET driver. It amplifies the CMOS-level signal from IC3 and is capable of driving up to 1.5A into the gates of the power FETs. A fast charge / discharge time is essential for highly efficient, and disaster-free operation of a class-D amplifier. C20 and C21 AC-couple the drive to the FETs. Schottky diodes, D4 and D5, restore the correct DC level at the gates while R20 - R23 ensure stability.

The Class-D push-pull output stage comprises FETs TR2 and TR3 and output-matching transformer, T2. Initially, I selected a large E-core transformer for T2. This ETD44 core worked well, and was used in the prototype. Unfortunately, it proved both expensive and difficult to reproduce. Finally, it was replaced by a toroidal design, which was easier to construct. The drain-to-drain impedance of the FETs is matched to 50Ω by the turns ratio of T2. A series of taps on the secondary allows the turns ratio of T2 to be changed, allowing the power delivered to the antenna to be selected via a front panel ceramic switch. The highest number of secondary turns provides the highest output power.

The DC supply is passed through an ammeter and current-sense resistor and is decoupled by C26 and C27. DC is applied to the centre tap on the primary of T2. L4 and C23 provide additional filtering.

The RF output passes from the secondary of T2 through transmit / receive relay, RL1. A second relay, RL2, has been included to terminate the receiver input when in transmit mode. These relays are rated at 12A, and have been tested at 136kHz with power levels of 1000W. Diode D10 is included to protect any semiconductors included in the external switching arrangements.

From the relays, the RF passes through a multi-element low-pass filter to the output. The LPF is essential for removing the high levels of harmonics which are present in the square-wave output from the amplifier. The T157 core used for L3 is rated to about 400W, while the polypropylene capacitors are all specified at 1kV and are capable of handling much higher power levels. The cut-off frequency of the filter is 200kHz, ensuring a very low insertion loss at 136kHz.

REFLECTED POWER PROTECTION

FORWARD AND REFLECTED power are detected by directional coupler, T1. A single wire passing through the centre of the toroid acts as a single-turn primary, while the secondary is a bifilar winding of 13 turns. The secondary produces outputs proportional to forward and reflected power. These AC signals are rectified by diodes D6 and D7. Preset potentiometers, RV4 and RV5, set the sensitivity. Switch S2 selects whether forward or reflected power is displayed on the meter.

Resistors R29 and R30 define the reference voltage at the non-inverting input of IC7, and hence set the trip point of the protection circuit. Under normal operation, pin 6 of IC7 is at 12V. When the voltage at the wiper of RV3 exceeds the voltage at pin 3, the output at pin 6 rapidly falls from 12V to zero. This circuit was adapted from a Motorola application note [2] and is very fast-acting. It is claimed to be capable of switching off the drive in about 10µs. The op-amp output is connected to the input of IC6, a 4538 dual-monostable. Once triggered, the output of the monostable changes from 0V to 12V. This voltage forward-biases D1, which causes the Set Direct function of the 4013 to shut down the device. The output of the 4538 also illuminates a front panel LED giving a visual indication of the cause of the shutdown. Having cut off the drive, the monostable maintains this condition for a period determined by R32 and C28, about 2.2s. The circuit resets automatically.

OVER-CURRENT PROTECTION

OVER-CURRENT protection has been implemented by utilising current-sense resistor, R25, with TR4 and opto-coupler IC5. When the current flowing through R25 causes a potential difference of 0.7V to be developed across it, the pnp transistor, TR4, will switch on. Current then flows through R38 and the diode contained within the opto-coupler.

When the LED forward current reaches 600µA, an internal Schmitt trigger causes the output voltage to fall rapidly from 12V to zero. This triggers the other half of the dual-monostable, IC6. To preserve the speed of the over-current trip, there are no decoupling capacitors around TR4 or IC5. Once again, the response time of this circuit is very fast and it can reduce the output to zero in about 10-20µs. The exact value of the trip point can be adjusted over a small range by RV6.

CONSTRUCTION

THE PCB SHOULD be assembled and tested before being fitted into an enclosure. Start by constructing the VXO and logic circuits, leaving the low-pass filter coils, transformer T2, and directional coupler T1, until last. The power FETs can be temporarily fitted for testing and then mounted permanently after testing is complete. The coils L2 and L3 in the low-pass filter are quite large and can be held in place using a little epoxy glue for extra support. When fitting inductors, ensure that the enamelled wire does not come into direct contact with the earth plane. This avoids high voltages arcing through the thin insulation and other damage due to abrasion. The primary of T1 is a single wire passing through the centre of the toroid. I used a small length of the inner conductor from RG58 coaxial cable.

The powder-coated ready-punched enclosure used in the prototype is available from H J Morgan Smith [3].

NEXT MONTH

TESTING IS COVERED next month, together with some ideas on antennas for LF. Some consideration is also given to what you might expect to work on LF, and what computing equipment you would need for more sophisticated modes. There is also a list of components.

REFERENCES

[1] PIC- or PC-controlled 0-6 MHz DDS VFO (AD9832). Johan Bodin, SM6LKM. **http://home4.swipnet.se/~w-41522/minidds/minidds.html**

[2] AR510: 'VSWR Protection of Solid State RF Power Amplifiers', by H O Granberg, *RF Design*, Feb 1991.

[3] H J Morgan Smith, sheet metal engineers. Tel: 01293 452 421. ♦